2.7 V to 5.5 V, 140 µA, Rail-to-Rail Voltage Output 10-Bit DAC in a SOT-23

Data Sheet **AD5310**

FEATURES

Single 10-bit DAC
6-lead SOT-23 and 8-lead µSOIC packages
Micropower operation: 140 µA @ 5 V
Power-down to 200 nA @ 5 V, 50 nA @ 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Reference derived from power supply
Power-on reset to 0 V
Three power-down functions
Low power serial interface with Schmitt triggered inputs
On-chip output buffer amplifier, rail-to-rail operation
$\overline{\text{SYNC}}$ interrupt facility
Qualified for automotive applications

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

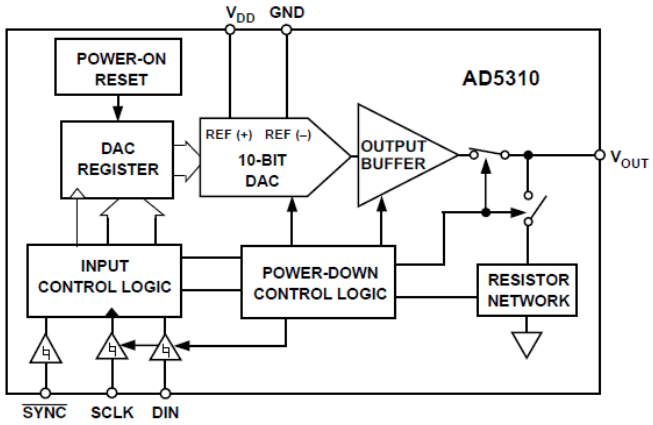


Figure 1.

GENERAL DESCRIPTION

The AD5310[1] is a single, 10-bit, buffered voltage output DAC that operates from a single 2.7 V to 5.5 V supply, consuming 115 µA at 3 V. Its on-chip precision output amplifier allows rail-to-rail output swing. The AD5310 utilizes a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE®, and DSP interface standards.

The reference for AD5310 is derived from the power supply inputs and, therefore, provides the widest dynamic output range. The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V and remains there until a valid write takes place to the device. The part contains a power-down feature, which reduces the current consumption of the device to 200 nA at 5 V and provides software-selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface.

The low power consumption of this part in normal operation makes it ideally suited for portable, battery-operated equipment. The power consumption is 0.7 mW at 5 V, reducing to 1 µW in power-down mode.

The AD5310 is one of a family of pin-compatible DACs. The AD5300 is the 8-bit version, and the AD5320 is the 12-bit version. The AD5300/AD5310/AD5320 are available in 6-lead SOT-23 packages and 8-lead µSOIC packages.

PRODUCT HIGHLIGHTS

1. Available in 6-lead SOT-23 and 8-lead µSOIC packages.
2. Low power, single-supply operation. This part operates from a single 2.7 V to 5.5 V supply and typically consumes 0.35 mW at 3 V and 0.7 mW at 5 V, making it ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a slew rate of 1 V/µs.
4. Reference derived from the power supply.
5. High speed serial interface with clock speeds of up to 30 MHz. Designed for very low power consumption. The interface only powers up during a write cycle.
6. Power-down capability. When powered down, the DAC typically consumes 50 nA at 3 V and 200 nA at 5 V.

[1] Patent pending; protected by U.S. Patent No. 5684481.

Rev. B
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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- AD5310: +2.7 V to +5.5 V, 140 µA, Rail-to-Rail Voltage Output 10-Bit DAC in a SOT-23 Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Technical Articles

- DDS Device Provides Amplitude Modulation

DESIGN RESOURCES

- AD5310 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

7/12—Rev. A to Rev. B

Updated Format ... Universal
Changes to Features ... 1
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Changes to AD5310 to ADSP-2101 Interface Section and Figure 27 ... 12
Updated Outline Dimensions ... 16
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Added Automotive Products Section ... 16

5/99—Rev. 0 to Rev. A

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; temperature range = −40°C to +105°C R_L = 2 kΩ to GND; C_L = 500 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	10			Bits	
Relative Accuracy			±4	LSB	See Figure 5
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design (see Figure 6)
Zero Code Error		5	40	mV	All 0s loaded to DAC register (see Figure 9)
Full-Scale Error		−0.15	−1.25	% of FSR	All 1s loaded to DAC register (see Figure 9)
Gain Error			±1.25	% of FSR	
Zero Code Error Drift		−20		µV/°C	
Gain Temperature Coefficient		−5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		6	8	µs	¼ scale to ¾ scale change (100 hex to 300 hex)
Slew Rate		1		V/µs	R_L = 2 kΩ; 0 pF < C_L < 500 pF (see Figure 19)
Capacitive Load Stability		470		pF	R_L = ∞
		1000		pF	R_L = 2 kΩ
Digital-to-Analog Glitch Impulse		20		nV-s	1 LSB change around major carry (see Figure 22)
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short-Circuit Current		50		mA	V_{DD} = 5 V
		20		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5		µs	Coming out of power-down mode, V_{DD} = 3 V
LOGIC INPUTS[2]					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = 5 V
V_{INL}, Input Low Voltage			0.6	V	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.4			V	V_{DD} = 5 V
V_{INH}, Input High Voltage	2.1			V	V_{DD} = 3 V
Pin Capacitance			3	pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		140	250	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		115	200	µA	V_{IH} = V_{DD} and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.05	1	µA	V_{IH} = V_{DD} and V_{IL} = GND
Power Efficiency					
I_{OUT}/I_{DD}		93		%	I_{LOAD} = 2 mA, V_{DD} = 5 V

[1] Linearity calculated using a reduced code range of 12 to 1011. Output unloaded.
[2] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	V_{DD} = 2.7 V to 3.6 V	V_{DD} = 3.6 V to 5.5 V		
t_1[3]	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	22.5	13	ns min	SCLK low time
t_4	0	0	ns min	$\overline{SYNC}$ to SCLK rising edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	50	33	ns min	Minimum $\overline{SYNC}$ high time

[1] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] See Figure 2.
[3] Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

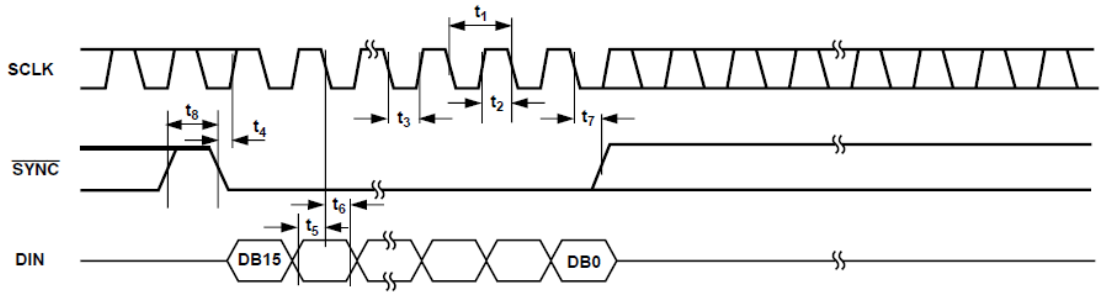


Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	+150°C
SOT-23 Package	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
µSOIC Package	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

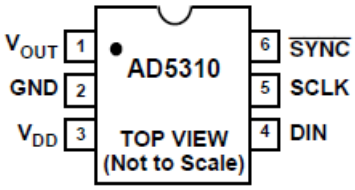


Figure 3. SOT-23

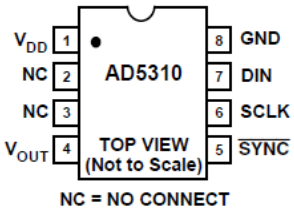


Figure 4. µSOIC

Table 4. SOT-23 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
2	GND	Ground Reference Point for All Circuitry on the Part.
3	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and V_{DD} should be decoupled to GND.
4	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
5	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 30 MHz.
6	$\overline{\text{SYNC}}$	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC.

TYPICAL PERFORMANCE CHARACTERISTICS

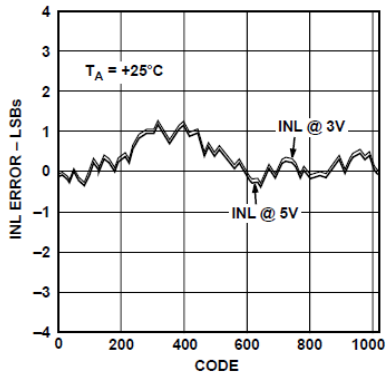


Figure 5. Typical INL

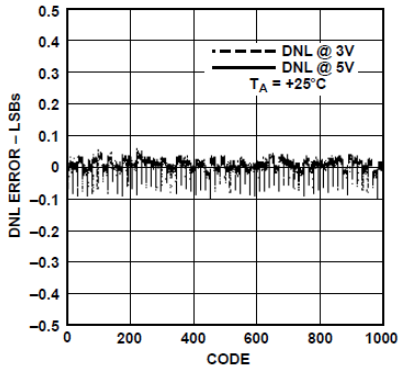


Figure 6. Typical DNL

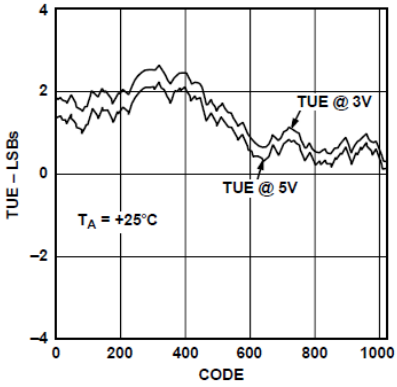


Figure 7. Typical Total Unadjusted Error

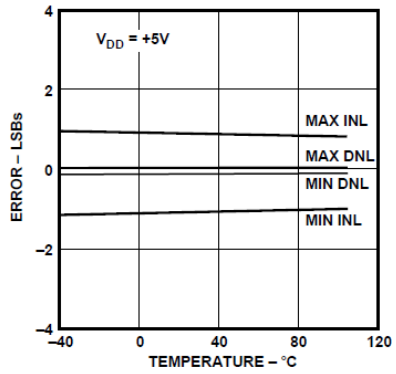


Figure 8. INL Error and DNL Error vs. Temperature

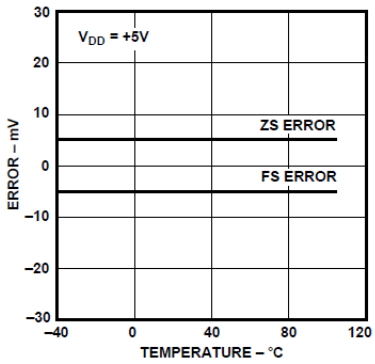


Figure 9. Zero Code Error and Full-Scale Error vs. Temperature

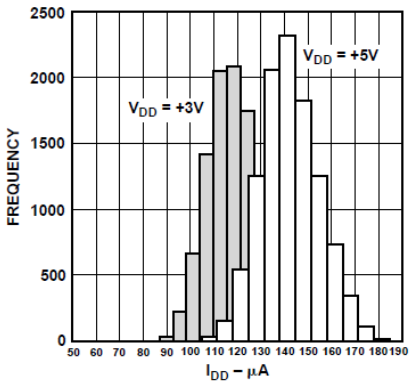


Figure 10. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

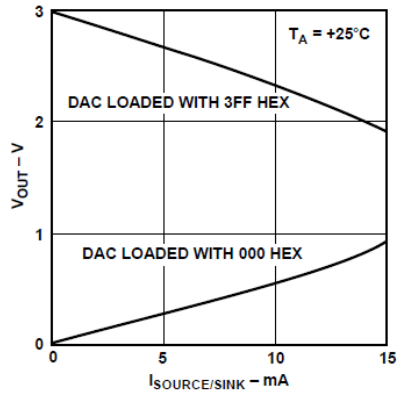


Figure 11. Source and Sink Current Capability with V_{DD} = 3 V

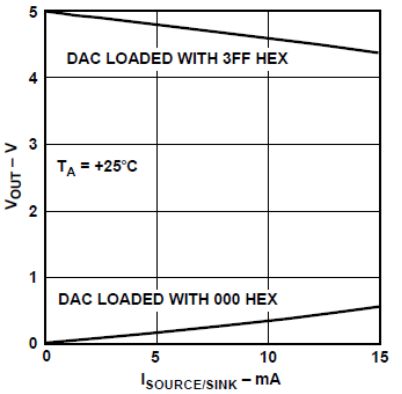


Figure 12. Source and Sink Current Capability with V_{DD} = 5 V

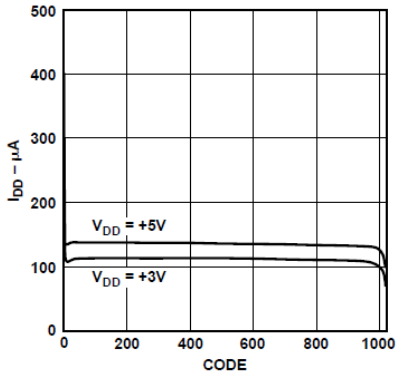


Figure 13. Supply Current vs. Code

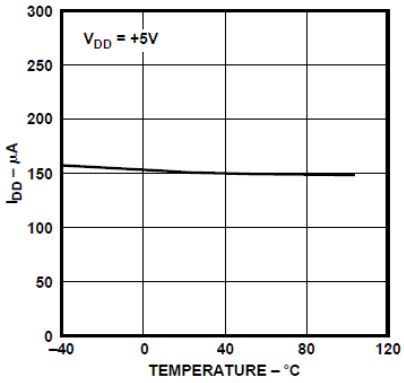


Figure 14. Supply Current vs. Temperature

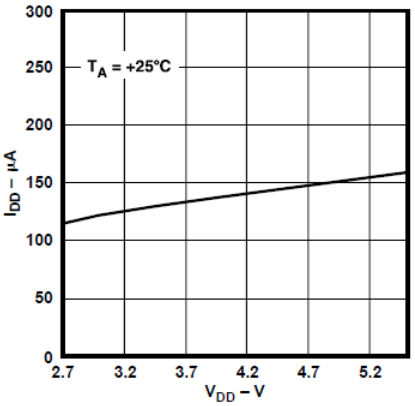


Figure 15. Supply Current vs. Supply Voltage

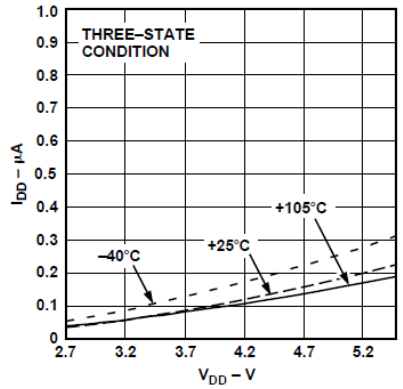


Figure 16. Power-Down Current vs. Supply Voltage

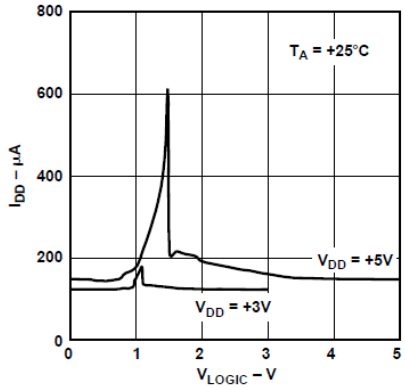


Figure 17. Supply Current vs. Logic Input Voltage

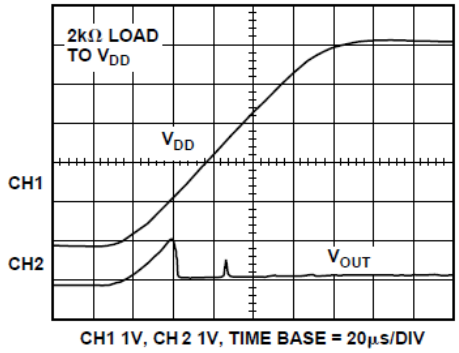


Figure 20. Power-On Reset to 0 V

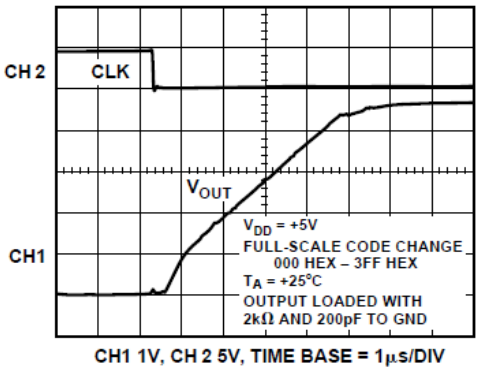


Figure 18. Full-Scale Settling Time

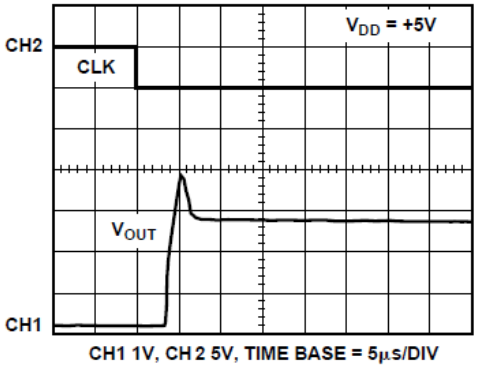


Figure 21. Exiting Power-Down (200 Hex Loaded)

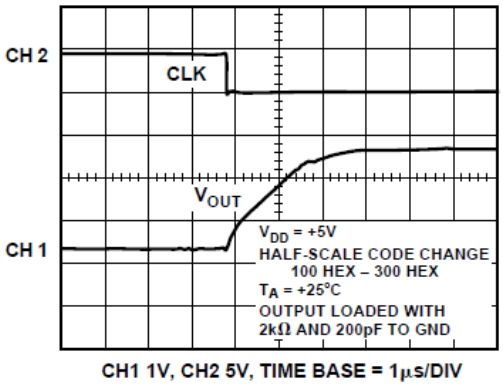


Figure 19. Half-Scale Settling Time

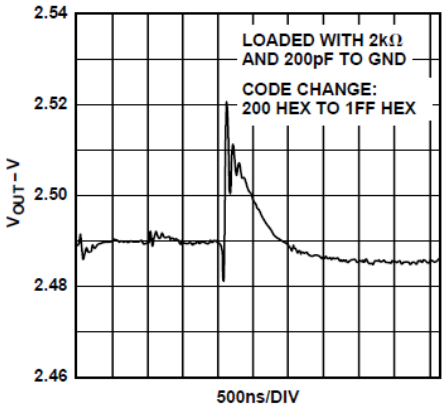


Figure 22. Digital-to-Analog Glitch Impulse

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 5.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 6.

Zero Code Error
Zero code error is a measure of the output error when zero code (000 hex) is loaded to the DAC register. Ideally, the output should be 0 V. The zero code error is always positive in the AD5310 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero code error is expressed in mV. A plot of zero code error vs. temperature is shown in Figure 9.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (3FF Hex) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. A plot of full-scale error vs. temperature is shown in Figure 9.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error that takes all the various errors into account. A typical TUE vs. code plot is shown in Figure 7.

Zero Code Error Drift
Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (1FF hex to 200 hex). See Figure 22.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

THEORY OF OPERATION

D/A SECTION

The AD5310 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (V_{DD}) acts as the reference. Figure 23 shows a block diagram of the DAC architecture.

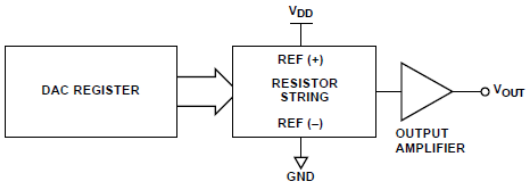


Figure 23. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{DD} \times \left(\frac{D}{1024} \right)$$

where D is the decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 1023.

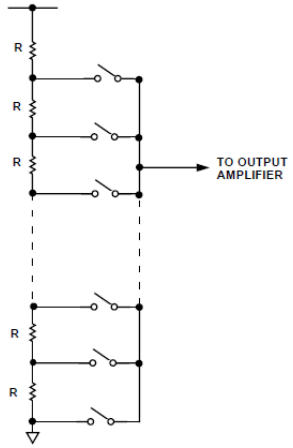


Figure 24. Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 24. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which results in an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 11 and Figure 12. The slew rate is 1 V/µs with a half-scale settling time of 6 µs with the output loaded.

SERIAL INTERFACE

The AD5310 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5310 compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2.4 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As previously mentioned, however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 25). The first two bits are don't cares. The next two bits are control bits that control which mode of operation the part is in (normal mode or one of the three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next 10 bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK. Finally, the last two bits are don't cares.

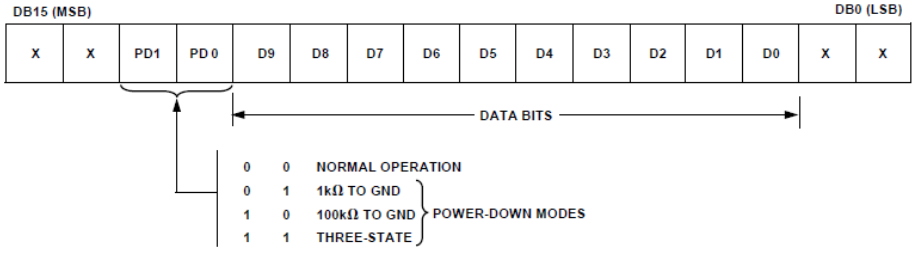


Figure 25. Input Register Contents

SYNC INTERRUPT

In a normal write sequence, the SYNC line is kept low for at least 16 falling edges of SCLK, and the DAC is updated on the 16th falling edge. However, if SYNC is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs (see Figure 28).

POWER-ON RESET

The AD5310 contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with 0s, and the output voltage is 0 V. It remains there until a valid write sequence is performed to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The AD5310 contains four separate modes of operation. These modes are software programmable by setting two bits (DB13 and DB12) in the control register. Table 5 shows how the state of the bits corresponds to the mode of operation of the device.

Table 5. Modes of Operation for the AD5310

Operating Mode	DB13	DB12
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
100 kΩ to GND	1	0
Three-State	1	1

When both bits are set to 0, the part works normally with its normal power consumption of 140 µA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage of knowing the output impedance of the part when the part is in power-down mode. There are three options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 26.

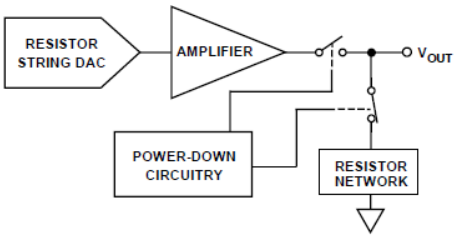


Figure 26. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and 5 µs for V_{DD} = 3 V (see Figure 21).

MICROPROCESSOR INTERFACING

AD5310 to ADSP-2101 Interface

Figure 27 shows a serial interface between the AD5310 and the ADSP-2101. The ADSP-2101 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

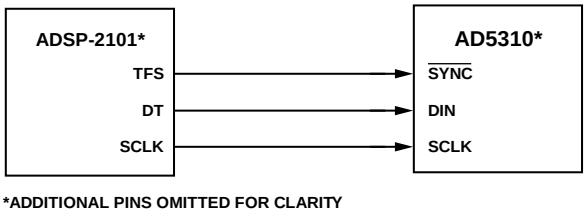


Figure 27. AD5310 to ADSP-2101 Interface

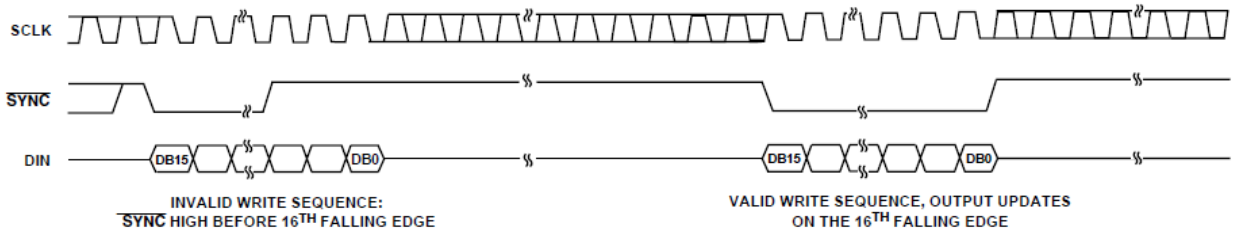


Figure 28. SYNC Interrupt Facility

AD5310 to 68HC11/68L11 Interface

Figure 29 shows a serial interface between the AD5310 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5310, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). With this 68HC11/68L11 configuration, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5310, PC7 is left low after the first eight bits are transferred, a second serial write operation is performed to the DAC, and PC7 is taken high at the end of this procedure.

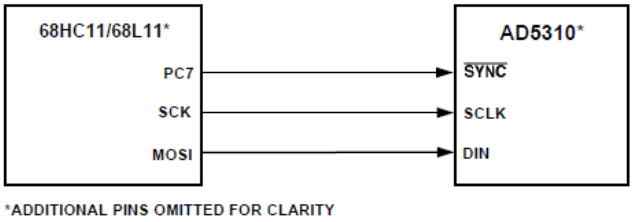


Figure 29. AD5310 to 68HC11/68L11 Interface

AD5310 to 80C51/80L51 Interface

Figure 30 shows a serial interface between the AD5310 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5310 while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5310, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/ 80L51 outputs the serial data in a format that has the LSB first. The AD5310 requires that the MSB of data be received first. The 80C51/80L51 transmit routine should take this into account.

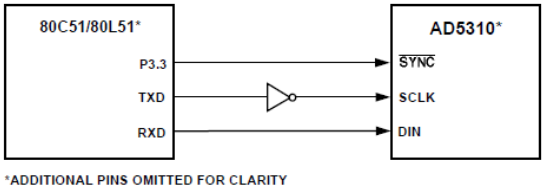


Figure 30. AD5310 to 80C51/80L51 Interface

AD5310 to MICROWIRE Interface

Figure 31 shows an interface between the AD5310 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5310 on the rising edge of the SK.

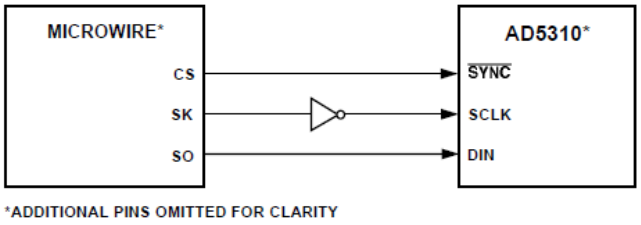


Figure 31. AD5310 to MICROWIRE Interface

APPLICATIONS INFORMATION

USING REF19x AS A POWER SUPPLY FOR AD5310

Because the supply current required by the AD5310 is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) to supply the required voltage to the part (see Figure 32). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (for example, 15 V). The REF19x outputs a steady supply voltage for the AD5310. If the low dropout REF195 is used, the current that it needs to supply to the AD5310 is 140 µA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

140 µA + (5 V/5 kΩ) = 1.14 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.3 ppm (11.5 µV) for the 1.14 mA current drawn from it. This corresponds to a 0.002 LSB error.

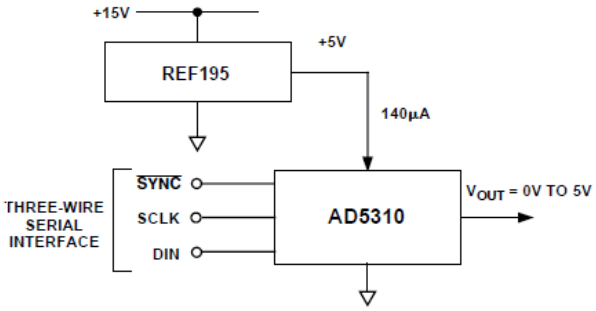


Figure 32. REF195 as Power Supply to AD5310

BIPOLAR OPERATION USING THE AD5310

The AD5310 is designed for single-supply operation but a bipolar output range is also possible using the circuit shown in Figure 33. This circuit results in an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier. The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{1024} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 1023).

With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{1024} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 000 hex corresponding to a −5 V output and 3FF hex corresponding to a +5 V output.

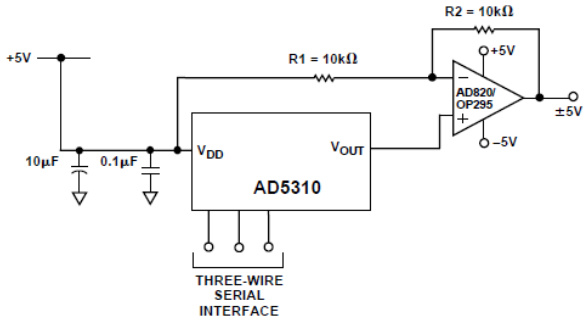


Figure 33. Bipolar Operation with the AD5310

USING AD5310 WITH AN OPTO-ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. Opto-isolators provide isolation in excess of 3 kV. Because the AD5310 uses a 3-wire serial logic interface, it only requires three opto-isolators to provide the required isolation (see Figure 34). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5310.

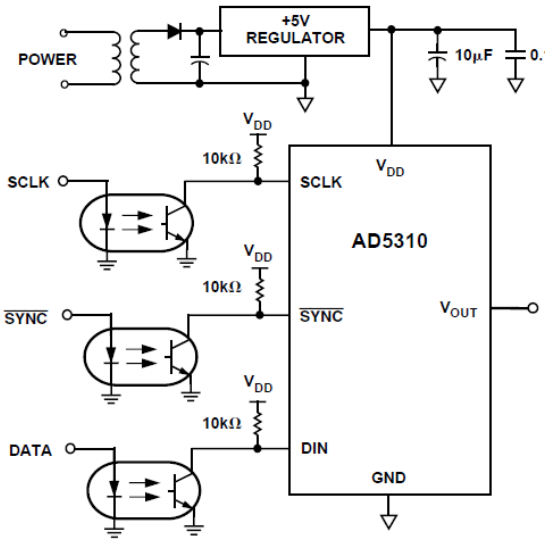


Figure 34. AD5310 with an Opto-Isolated Interface

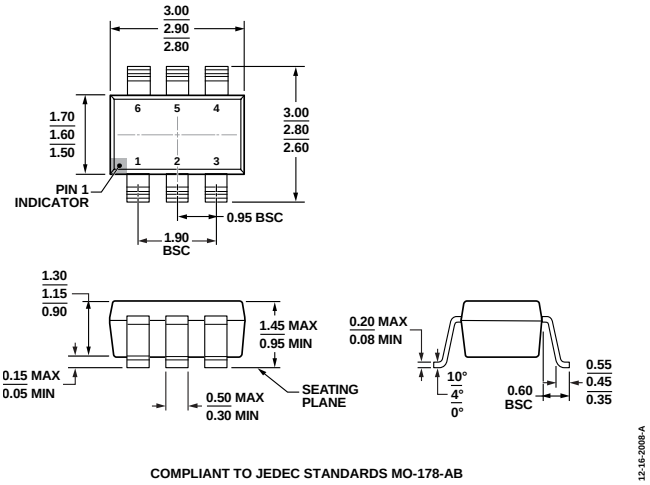
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5310 should have separate analog and digital sections, each having their own area of the board. If the AD5310 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5310.

The power supply to the AD5310 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), such as is the case with common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

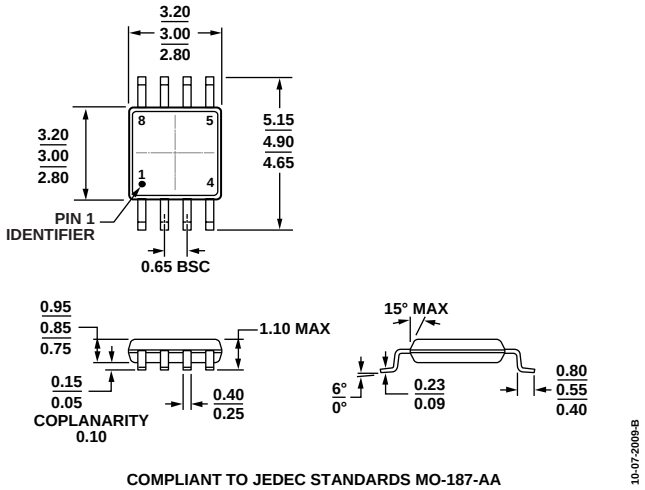
The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the micro-strip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 35. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding Information
AD5310BRTZ-REEL	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310BRTZ-REEL7	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310BRTZ-500RL7	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310BRT-REEL	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310BRT-REEL7	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310BRT-500RL7	–40°C to +105°C	6-Lead SOT-23	RJ-6	D3B
AD5310WBRTZ-REEL7	–40°C to +105°C	6-Lead SOT-23	RJ-6	DJW
AD5310BRMZ	–40°C to +105°C	8-Lead MSOP	RM-8	D3B
AD5310BRMZ-REEL7	–40°C to +105°C	8-Lead MSOP	RM-8	D3B
AD5310BRM	–40°C to +105°C	8-Lead MSOP	RM-8	D3B
AD5310BRM-REEL	–40°C to +105°C	8-Lead MSOP	RM-8	D3B

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD5310WBRTZ-REEL7 model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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